Technical Brief

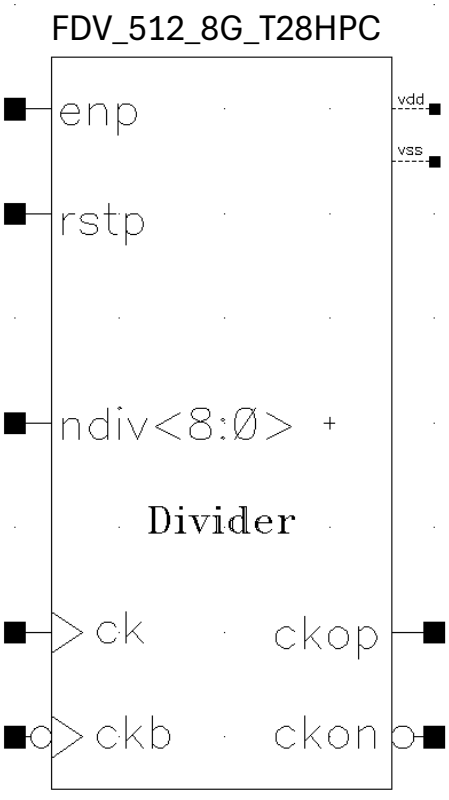
Kamaten Technology Incorporated

COMPACT DIGITAL FREQUENCY DIVIDERS

Overview

Kamaten frequency dividers reduce input digital signal (clock) frequency and can be set to any integer division ratio from 1 to 8, 64, 512 or 4096. Input and output clock signals are differential, all input, output and control signals are CMOS. **Dividers have very compact footprint**. Inductors are not used, reducing area and electromagnetic interference. Dividers are intended for use in frequency converting and synthetizing systems, requiring broad range of division ratios with full range coverage.

Symbol View



Symbol view is exemplar for high frequency version of 1:1:512 divider. Other dividers have identical symbol views except name and bit count on “ndiv<N:0> input. For instance, low power 1:1:64 divider will be FDV_64_2G_T28HPC with “ndiv<5:0>”.

Highlights

- Division ratio: any integer from 1 to 8/64/512/4096
- Maximum input frequency 2GHz – 8GHz (A)
- Typical consumption: 2 – 4mA at 1GHz (A)

  scales with frequency
- Duty cycle at output 50±5%
- Differential CMOS clock input and output signals
- Power down mode
- Bypass mode
- Low leakage current
- Typical power supply voltage 900mV
- Operational temperature: -40°C to +110°C
- Footprints:

  high frequency 1:1:512 -- 52 x 30 µm

  low power 1:1:64 -- 32 x 15 µm
- Process: TSMC 28nm HPC/HPC+;

  can be ported to other nodes on request

(A) – depending on design version and division ratio

Kamaten Technology Incorporated
Ottawa, Ontario Canada
info@kamaten.com