Data Sheet

Kamaten Technology Incorporated

PRBS71531HS-T28HPC: 32GBps PSEUDO RANDOM BIT SEQUENCE GENERATOR/CHECKER

Description

This unit generates and checks Pseudo Random Bit Sequence (PRBS) of 7, 15 or 31 order, up to 32Gbps. It can work as Generator only, Checker/Counter only or both simultaneously. In error checking mode unit may output PRBS signal, always error free. Embedded 10-bit error counter is accurate: no double counts or omissions regardless of error sequence or frequency of occurrences. Error count may start, stop or be reset at any time with no need to stop or reset the entire unit. Error count range is expandable (see Application Note). Indicator signal facilitates switching between Generator and Checker mode. Footprint is small, no inductors are used minimizing area and EM interference. Simple control interface, with low frequency asynchronous signals only. Unit is designed in TSMC 28HPC/HPC+ process. Design may be ported to more advanced process nodes.

Features

- PRBS order: 7, 15 or 31 based on formulas: **X1=X6^X7; X1=X14^X15; X1=X28^X31**.
- Full bit rate at input and output is up to 32Gbps.
- Generator and Checker functions; will output error free PRBS while in error checking mode.
- Accurate error count: no omissions or double counts.
- Full rate CMOS differential input data, centered with half-rate CMOS differential input clock.
- Full rate CMOS differential output data, aligned with half-rate CMOS differential output clock.
- Accurate embedded 10-bit error counter, externally expandable (see AN for details).
- Low frequency asynchronous CMOS control interface.
- Supply voltage: 0.9V.
- Power down mode.
- Typical power consumption: 80mA at 32Gbps in simultaneous Generator and Checker mode; scales with bit rate.
- Indicator signal facilitating switching between Generator and Checker mode.
- Operational temperature range: -40C to +110C.
- Footprint: 65 x 140 um.
- Process: TSMC 28nm HPC/HPC+, portable to more advanced processes.

Applications

Unit is intended for testing of communication channels and clock/data recovery systems. Helps to verify functionality and evaluate channel and system quality and efficiency by measuring bit error rates. Unit fits well with Design for Test (DFT) approach and makes an irreplaceable element of advanced Built-in Self Test (BIST) systems.

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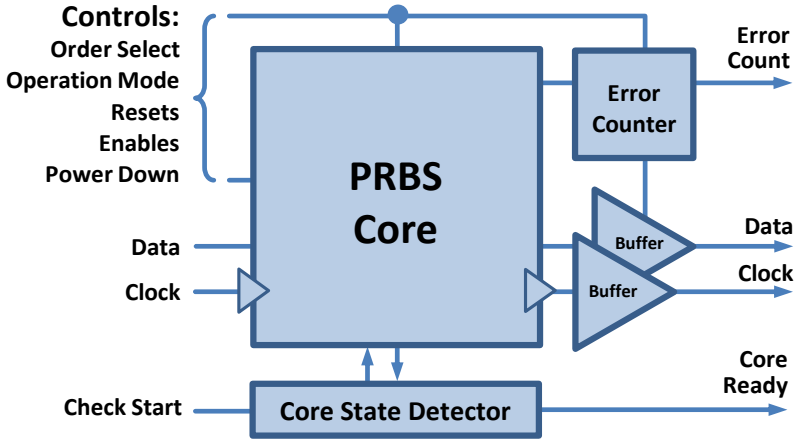
Operational Ratings

- Power Supply Voltage 0.85 – 0.95V
- Input Voltage 40 – 950mV
- Operating Temperature Range -40C/+110C
- Maximum Input Clock Frequency 16.4GHz
- Maximum Input Data Rate 32.8Gbps
- Error Counter Depth 2^10-1 (10-bit) extendable

Block Diagram



Basic Block Diagram

Operating Conditions

Parameter	Units	Value MIN	Value TYP	Value MAX	NOTES
Power supply voltage	mV	850.00	900.00	950.00	
Temperature (junction)	C	-40.00	40.00	120.00	
Clock frequency at input	GHz			16.40	
Data rate at input	Gbps			32.80	
Clock transition time at input, 20/80	ps			5.00	
Data transition time at input, 20/80	ps			5.00	
Clock/data low voltage at input	mV			40.00	
Clock/data high voltage at input	mV	Vdd-40.0			
Clock Duty Cycle Distortion (DCD) at input	%	-5.00		5.00	
Clock Skew at input	%	-5.00		5.00	
Setup Time at input (Tsu)	ps			7.00	*Tck-(Tsu+Th) makes the input data window. Clock sampling edges may move within this window*
Hold Time at input (Th)	ps			5.00	
Capacitive load at output	fF			25.00	In demo TB includes inverter input (about 17fF at Vdd/2) and 8fF metal routing for a total ~25fF
Rising/falling time, control signals	ps			100.00	Detailed timing is provided in Application Note

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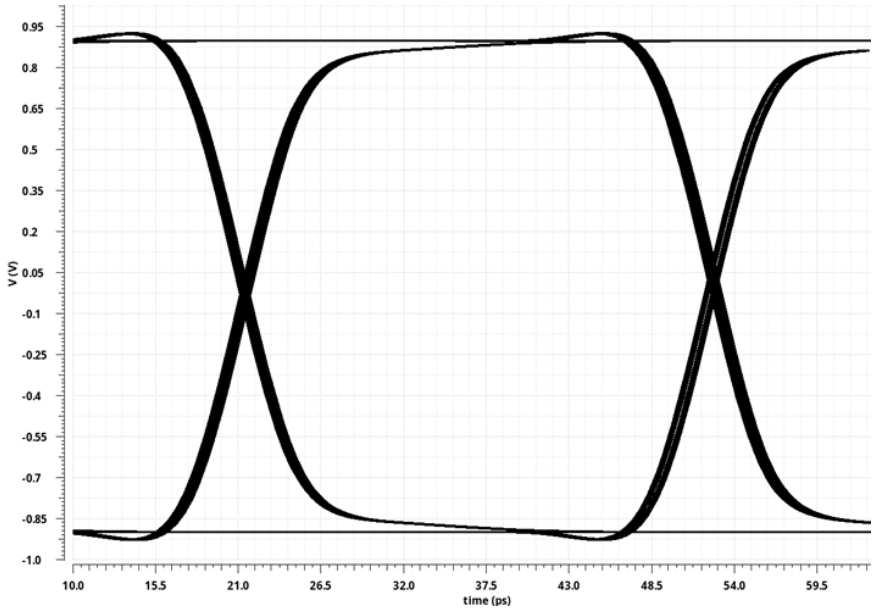
Electrical Characteristics

Parameter	Units	Value			NOTES
		MIN	TYP	MAX	
Data Rate at input	Gbps			32.8	*+110C/0.85V/SlowSlow*
Data Rate at Output	Gbps			32.8	*+110C/0.85V/SlowSlow*
Power Supply Current, active	mA		80.00	100.0	*Max at +110C/0.95V/FastFast*
Power Supply Current, powerdown	mA		0.20	1.5	*Max at +110C/0.95V/FastFast*
Clock/Data Transition Time at Output, 20/80	ps		6.00	8.0	*Max at +110C/0.85V/SlowSlow, Load ~25fF*
Clock to Output Data (Clock to Q)	ps	10.00	20.00	30.0	
Input Capacitance Data, approximate	fF		30.00	35.0	*Includes metal routing (~30-40%) and CMOS buffers input (~60-70%)*
Input Capacitance Clock, approximate	fF		50.00	60.0	

Typical Differential Data Eye at Output



Conditions:

+40C/0.9V/Typical, 32Gbps,

Cload ~25fF, PRBS-15

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