Data Sheet

Kamaten Technology Incorporated

PLL-INTN8G-T28HPC: GENERAL USE INTEGER-N 4GHz HYBRID PHASE LOCKED LOOP

Description

This Integer-N Hybrid (Digitally Aided Analog) PLL generates clock signals within broad frequency range. Division coefficients of the embedded input and feedback dividers can be set to any integer between 1 and 64 or may be bypassed to save power. Higher order dividers and/or pre-scalers are optional. Output clock may be 8- or 4-phase set by the user. Disabling 4 out of 8 output buffers also saves power. With use of external frequency multipliers, the output clock frequency may be doubled or quadrupled. User controlled embedded control register allows setting frequency division, loop bandwidth, phase margin, peaking. PLL has reference spur reduction functions also controlled by the control register. The control register has serial and parallel interfaces. This PLL has very short lock time, lock indicator signal and power-up sequence support signals. **Footprint is compact and no off-chip components are needed**. This PLL has Analog Test Bus (ATB) as a Design for Test (DFT) feature.

Features

- Output frequency range: 500MHz ÷ 2GHz
- Reference clock frequency range: 8MHz ÷ 2GHz
- User-set 4 or 8 output clock phases
- Loop bandwidth 60kHz - 180MHz, with phase margin $\geq$50°
- Output clock duty cycle 50 $\pm$5%
- Typically locks within 150 reference clock cycles
- Simple power-up sequence facilitated by indicator output signals
- All digital aid functions are embedded, minimum external control is required
- Embedded control register with serial and parallel interfaces
- Input for external ROM storing multiple pre-set states
- Typical supply voltage 900mV
- All input and output signals are CMOS
- Typical power consumption: 2.6mA at 1GHz, scales with VCO frequency
- Low leakage power down mode
- Operational temperature: -40°C to +110°C
- Footprint: 150 x 200 µm
- **Does not require any off-chip components**
- Design For Test (DFT) enabled by embedded Analog Test Bus (ATB)
- Process: TSMC 28nm HPC/HPC+, **design can be ported to other nodes**

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Applications

This general purpose PLL generates and synthetizes clock signals for a broad range of applications, such as telecommunication, consumer, automotive, industrial etc., where compact footprint, low power, very fast locking and high functional flexibility are needed while use of external components should be avoided.

Operating Conditions

Parameter	Units	Value			NOTES
		MIN	TYP	MAX	
Power supply voltage	mV	850.00	900.00	950.00	
Temperature (junction)	C	-40.00	40.00	110.00	
Clock frequency at input	GHz	0.08		2.00	
Clock transition time at input, 20/80	ps		5.00	10.00	
Clock low voltage at input	mV			40.00	
Clock high voltage at input	mV	Vdd-40.0			
Clock Duty Cycle Distortion (DCD) at input	%	-5.00		5.00	
Clock Skew at input	%	-5.00		5.00	
Capacitive load at output	fF			25.00	
Rising/falling time, control signals	ps			100.00	*Detailed timing requirements found in the Application Note*

Operational Ratings

Power Supply Voltage	0.85 ÷ 0.95V	Operating Temperature Range	-40°C ÷ +110°C
Input Voltage	(Vdd-40) ÷ 950mV	Maximum Input Clock Frequency	2GHz

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Electrical Characteristics

Parameter	Units	Value MIN	Value TYP	Value MAX	NOTES
Power supply current, active	mA		2.60	3.5	*Fout=1GHz, 4-phase output clock, M divider bypassed*
Power supply current, powerdown	uA		20.00	100.0	*Max at +110C/0.95V/FastFast*
Clock transition time at output, 20/80	ps		6.00	8.0	*Max at -40C/0.85V/SlowSlow, Load ~25fF*
Capacitance at clock input	fF		30.00	35.0	*Includes metal routing capacitance (~30-40%) and CMOS buffers input capacitance (~60-70%)*
Fundamental reference spur	dB		60.00		*Fvco=1GHz, N=40, M=1, (Fref=25MHz), Kvco~400MHz/V, with partial spur reduction engaged*

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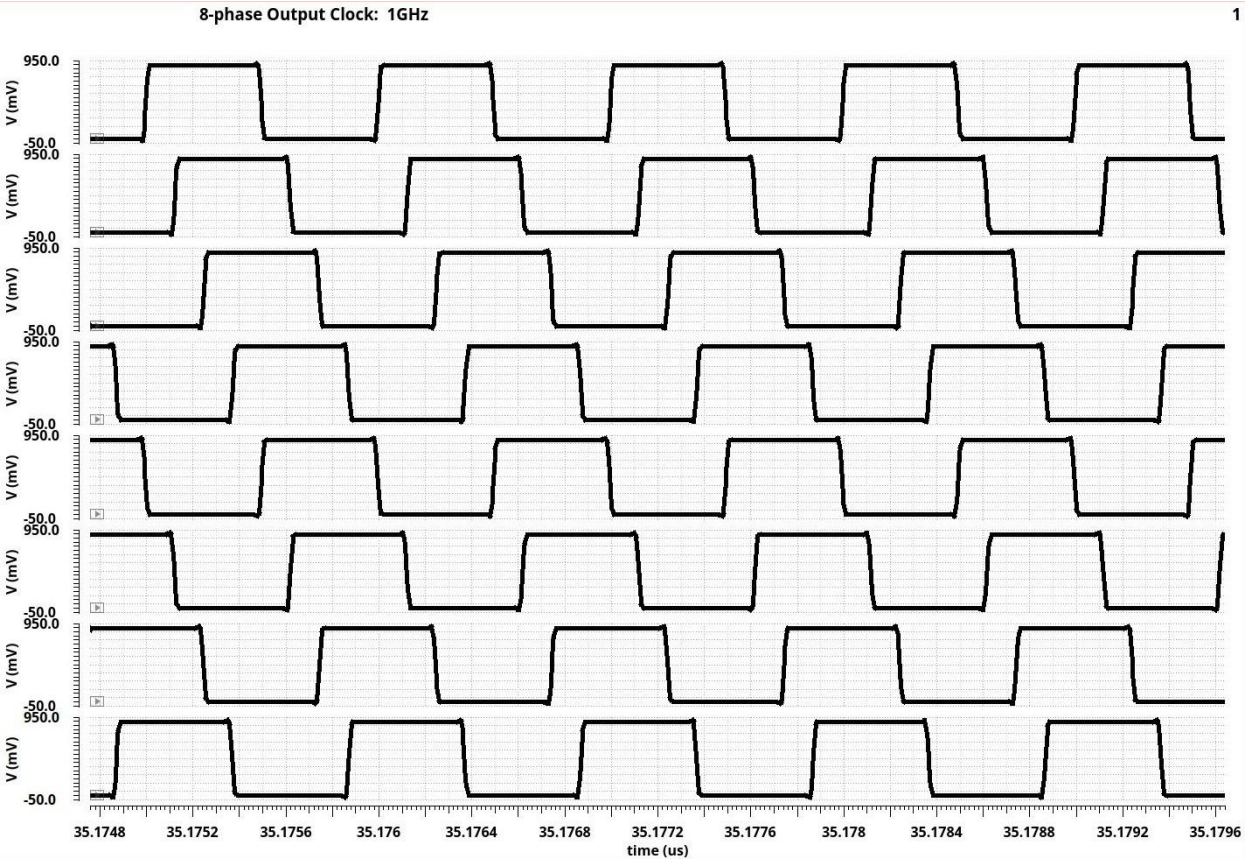
Typical 8-phase Clock at Output



Conditions:

+40C/0.9V/Typical,

Fout = 1GHz,

Cload ~25fF

Terminology

Fout or Fvco – output clock frequency [Hz]
Fref – reference clock frequency at reference clock inputs [Hz]
Kvco – VCO gain [Hz/V]
Icp – charge pump current [µA]
BW – loop bandwidth [Hz]
Peak – peaking [dB]

N – frequency divider in the feedback path (integer)
M – reference clock frequency divider: Fvco/N = Fref/M (integer)
RLF – loop filter resistor value [Ohm]
Kicp – charge pump current multiplier (integer)
PM – loop phase margin [deg]