Technical Brief

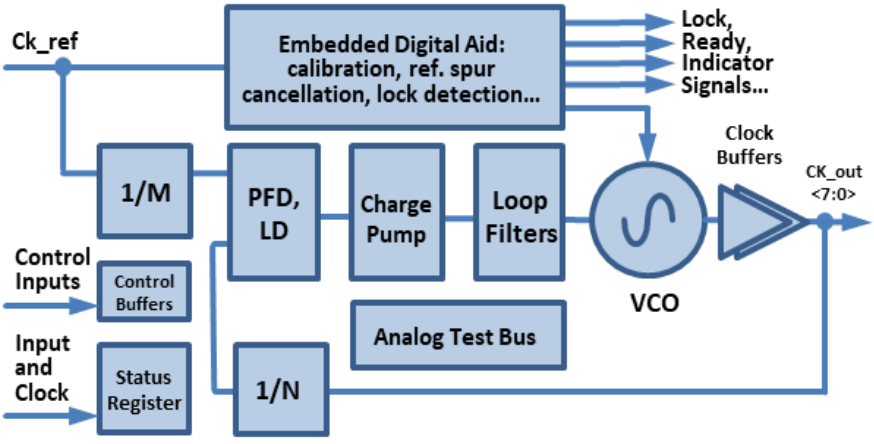
Kamaten Technology Incorporated

GENERAL USE INTEGER-N 4GHz HYBRID PHASE LOCKED LOOP

Overview

Kamaten Integer-N Hybrid (Analog with Digital Aid) PLL generates clock signals within broad frequency range. Division coefficients of the input and feedback dividers can be set to any integer between 1 and 64. Output clock is 8- or 4-phase, set by the user. Flexible, user-set configuration allows for controlling frequency division, bandwidth, phase margin, peaking and reference spur reduction functions. PLL lock time is short, power-up sequence is simple, supported by lock indicator signal and power-up sequence aid indicators. All digital aid functions are embedded. Footprint is compact and no off-chip components are needed.

Block Diagram



Highlights

- Output frequency range: 500MHz – 2GHz
- Loop bandwidth 60kHz – 180MHz
- 8 or 4 phase output clocks
- Output clock duty cycle 50 ±5%
- Typically locks within 150 reference clock cycles
- Simple power-up sequence
- Lock indicator signal
- Power-up sequence support indicator signals
- All digital aid functions are embedded
- User controlled reference spur reduction functions
- Serial and parallel control interface with internal status register. User configured pre-set states ROM
- All CMOS input and output signals
- Typical power supply voltage 900mV
- Typical consumption: 2.6mA at 1GHz VCO output; scales with VCO frequency
- Low leakage in power down mode
- Operational temperature: -40°C to +110°C
- Footprint: 200 x 150µm
- No off-chip components
- Analog Test Bus for DFT
- Process: TSMC 28nm HPC/HPC+; can be ported to other nodes

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