Technical Brief

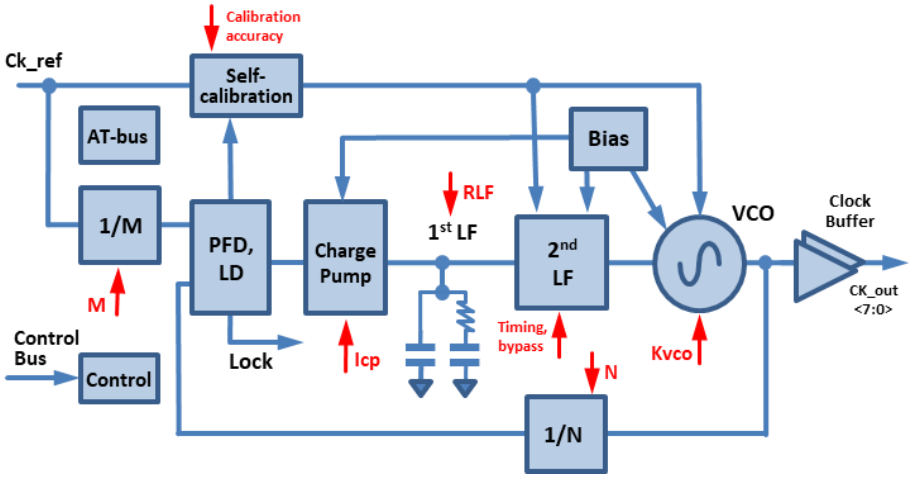
Kamaten Technology Incorporated

GENERAL USE INTEGER-N PLL

Overview

Kamaten Integer-N PLL synthetizes clock signals within broad frequency range. Division coefficients of the input and feedback dividers can be set to any integer between 1 and 64. Additional dividers or pre-scalers are optional. Output clock is 8-phase or 4-phase, set by the user. Flexible, user-set configuration allows for controlling frequency division, bandwidth, phase margin, peaking and reference spur. PLL is characterized by fast lock time and has lock indicator signal. Footprint is compact and no off-chip components are needed.

Block Diagram



Highlights

- Output frequency range: 500MHz – 2GHz
- 8 or 4 phase output clocks
- Output clock duty cycle 50 ±5%
- Typical lock within 150 reference cycles
- Lock indicator signal
- CMOS levels at all inputs and outputs
- Synchronous serial and asynchronous parallel control interface
- Typical supply voltage: 900mV core, 1.8V or 2.5V at in/out – optional
- Typical consumption: 8mA at 500MHz VCO output, scales with frequency
- Power down mode
- Operational temperature: -40C to +110C
- Footprint: 200 x 250 um
- Process: TSMC 28nm HPC/HPC+, can be ported to any other node

All information is subject to change

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