Technical Brief

Kamaten Technology Incorporated

PRBS-31: 32GBps PSEUDO RANDOM BIT SEQUENCE GENERATOR/CHECKER

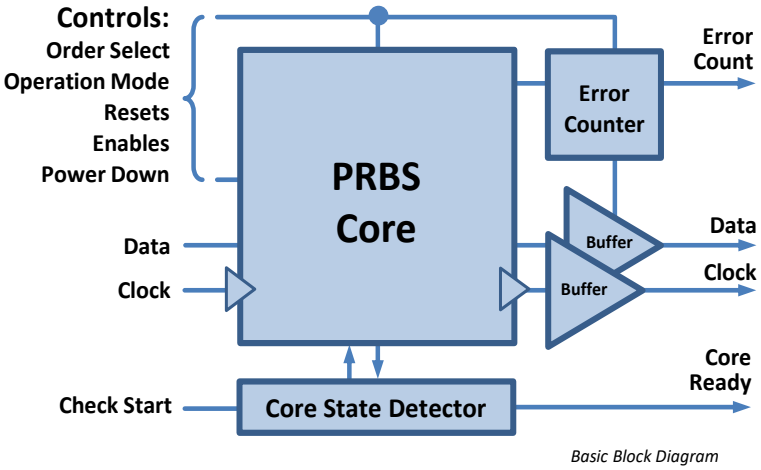
Overview

This unit generates and checks Pseudo Random Bit Sequence (PRBS) of 31 order, up to 32Gbps. Error count is accurate: no double counts or omissions regardless of error sequence or frequency of occurrence. Can be used as Generator, Checker or both. No inductors are used minimizing area and EM interference. Simple control interface, with low frequency asynchronous signals only.

Highlights

- PRBS order: 31 based on formula: **X1=X28^X31**
- Full bit rate at input and output up to 32Gbps
- Generator, Checker and Counter functions
- Accurate error count: no omissions or double counts
- Full rate CMOS differential input data, centered with half-rate CMOS differential clock
- Full rate CMOS differential output data, aligned with half-rate CMOS differential clock
- Asynchronous low frequency CMOS control interface
- Supply voltage: 0.9V
- Typical power consumption: 70mA at 32Gbps in simultaneous Generator and Checker mode; scales with bit rate
- Power down mode
- Error counter ready indicator signal
- Operational temperature range: -40C to +110C
- Footprint: 65 x 70 um
- Process: TSMC 28nm HPC/HPC+, portable to more advanced processes

Basic Block Diagram



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