

# Technical Brief

## SLAVE GENERATOR TOOL

### Overview

This Slave Generator is a powerful code generation tool. Given a set of input files it produces the following output files:

- ❖ Documentation in .html, .csv and .txt formats;
- ❖ Output in .xml for compatibility with 3rd vendors;
- ❖ System Verilog Code consisting of:
  - Address Decoders,
  - Slave Modules,
  - vh files containing the defines.
  - testbench and testcase generation.
  - software drivers design (additional files required).

### Highlights

- APB Interface connectivity
- User friendly interface
- Flexible Address & Data Bus Sizes
- Interrupt tree generation

All information is preliminary

### Block Diagram

