Technical Brief

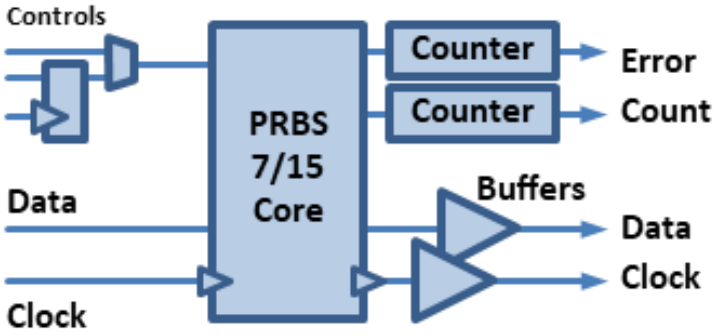
Kamaten Technology Incorporated

PRBS-7/15, 32GBPS PSEUDO RANDOM BIT SEQUENCE UNIT

Overview

This PRBS unit generates and/or checks PRBS-7 or PRBS-15 signals of up to 32Gbps rate. Two error counters, - separately for even and odd bits with separate enable, reset inputs and overflow outputs. Accurate error count, each error counts only once, no echo error counts regardless of error sequence or frequency of occurrence. Slim footprint, no inductors are used minimizing area and EM interference. Control interface is simple, limited support is required from digital side.

Block Diagram



Highlights

- PRBS order: 7 or 15 (X1=X6^X7 or X1=X14^X15)
- Bit rate up to 32Gbps in and out
- Independent generator and checker functions: checks, generates or both simultaneously
- Accurate error count: each error counts only once
- Separate error counters with overflow indicators for even and odd bits with independent enable and reset
- Accepted at input: full rate differential data centered with half-rate differential clock
- Produced at output: full rate differential data aligned with half-rate differential clock
- Synchronous serial, asynchronous parallel control interface
- CMOS levels at all inputs and outputs
- Supply voltage: 900mV core, 1.8/2.5V at in/out optional
- Typical consumption: 80mA at 32Gbps, generator + checker mode, scales with bit rate
- Power down mode
- Temperature range: -40C to +110C
- Footprint: 50 x 60 um
- Process: TSMC 28nm HPM, HPC/HPC+, can be ported to more advanced nodes

All information is preliminary

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