# Technical Brief

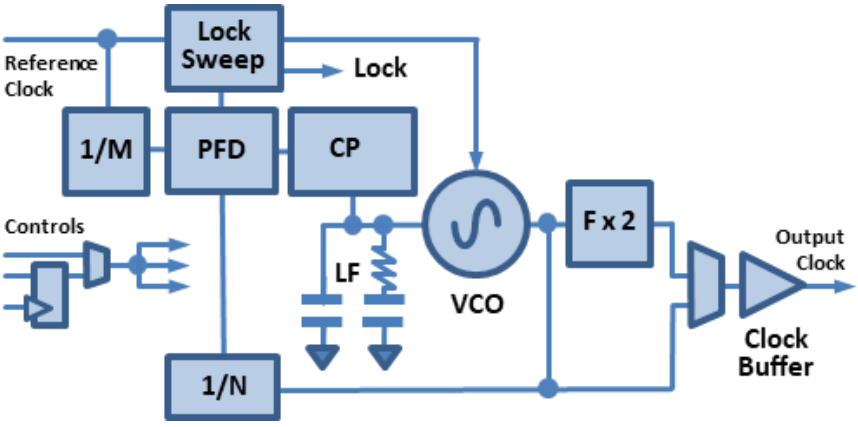
Kamaten Technology Incorporated

## INTEGER-N PLL FOR ASIC AND uC APPLICATIONS

## Overview

This Integer-N PLL synthetizes clock signals within broad frequency range. Input and feedback dividers with division coefficients of any integer 1 to 32, prescaler and output divider optional. Output clock is lower frequency quadrature or double frequency differential, - frequency doubler at output is optional. Fast lock time, lock indicator signal. Modest footprint and power consumption.

## Block Diagram




## Highlights

- Output frequency range:
  400MHz – 2GHz quadrature
  800MHz – 4GHz differential
- Frequency lock within 150 reference frequency cycles after reset
- Lock indicator signal
- CMOS levels at all inputs and outputs
- Synchronous serial and asynchronous parallel control interface
- Supply voltage: 900mV core, 1.8V or 2.5V at in/out – optional
- Typical consumption:12-14mA with 400MHz differential output, scales with output frequency
- Power down mode
- Temperature range: -40C to +110C
- Footprint: 100 x 140 um
- Process: TSMC 28nm HPM, HPC/HPC+, can be ported to more advanced nodes

All information is preliminary

**Kamaten Technology Incorporated**
Ottawa, Ontario Canada
info@kamaten.com

613-863-8024
www.kamaten.com