Technical Brief

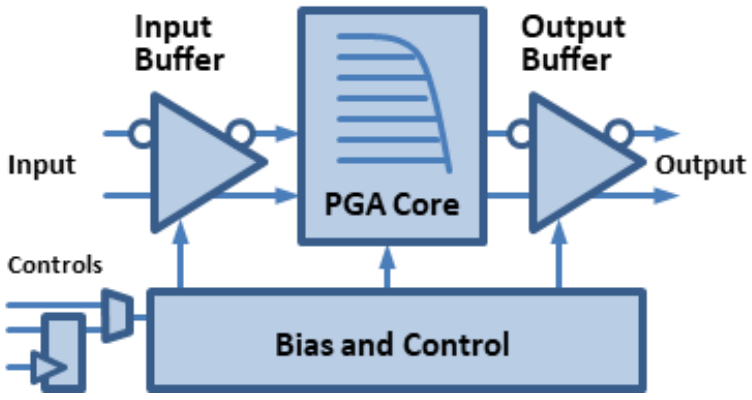
Kamaten Technology Incorporated

PROGRAMMABLE GAIN AMPLIFIER

Overview

This PGA has typical -3dB bandwidth of 24GHz and controlled flat gain 0dB to 12dB with 1dB granularity. Input common mode voltage is accepted from the driver. Output common mode voltage is controlled by internal DAC independently from input. Low input capacitance and input referred noise. Output is buffered to drive increased capacitive load. Internal DAC controls offset voltage (DCD).

Block Diagram



Highlights

- 3dB bandwidth: 24GHz
- Flat (DC) gain range: 0dB to 12dB, by 1dB
- Independently set input and output common mode voltages
- Output swing up to 400mVppd (Vout_cm=midrail, non-linearity <1dB)
- Input single-ended capacitance: <40fF
- Load single-ended capacitance up to 140fF
- Synchronous serial, asynchronous parallel control interface
- Supply voltage: 900mV core, 1.8V or 2.5V at in/out optional
- Typical consumption: 20-22mA at 25Gbps and maximum capacitive load
- Power down and mute mode
- Temperature range: -40C to +110C
- Footprint: 100 x 400 um
- Process: TSMC 28nm HPM, HPC/HPC+, can be ported to more advanced nodes

All information is preliminary

Kamaten Technology Incorporated
Ottawa, Ontario Canada
info@kamaten.com

613-863-8024
www.kamaten.com