Technical Brief

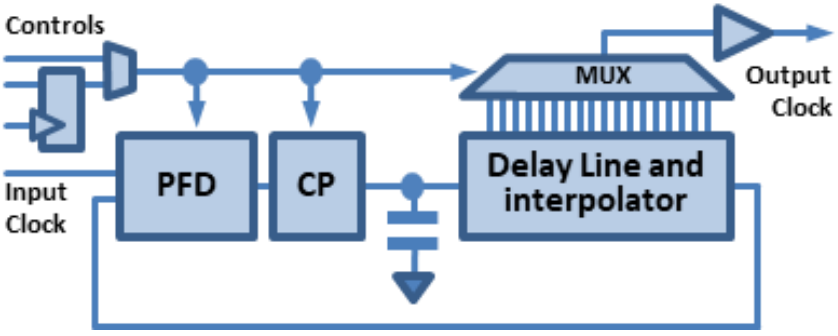
Kamaten Technology Incorporated

32-PHASE DELAY LOCKED LOOP

Overview

This simple DLL locks single period of clock and slices it into 32 phases one of which is available at the output. Accurate and steady phase relationship, modest power and slim footprint. Compatible with our PRBS generator/checker facilitating stable clock and data centering at input of the PRBS unit.

Block Diagram



Highlights

- Frequency range: 24GHz – 32GHz
- Granularity: 32 phases (11.25 degrees)
- CMOS levels at all inputs and outputs
- Supply voltage: 900mV core, 1.8V or 2.5V at in/out – optional
- Typical consumption: TBD
- Power down mode
- Temperature range: -40C to +110C
- Footprint: TBD
- Process: TSMC 28nm HPM, HPC/HPC+, can be ported to more advanced nodes

All information is preliminary

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