Technical Brief

Kamaten Technology Incorporated

# 100G REED-SOLOMON FORWARD ERROR CORRECTION (FEC) IP

## Overview

This IP supports the following modes as in IEE 802.3b:

Reed Solomon FEC RS (528,514,7,10) with FEC bypass and error correction.

Reed Solomon FEC RS (544,514,15,10) with FEC bypass and error correction.

The RS-FEC core implements the FEC encoder and decoder per section 91.5.2.7/91.5.3.3 of the IEEE 802.3bj.

The encoder accepts sixteen 10-bit words (160 bit total) on every positive edge of the clock when vld is asserted. Additional sof and eof inputs are used to mark the beginning and the end of the RS-FEC frame. Note that only two code words from the last 16 code words carry user data. The rest 14 of the last code will be overwritten with the calculated parity code words. RS-FEC frame size is 33 clock cycles in a case of RS(528,514,7,10) mode and 34 clock cycles in a case of RS(544,514,15,10) mode.

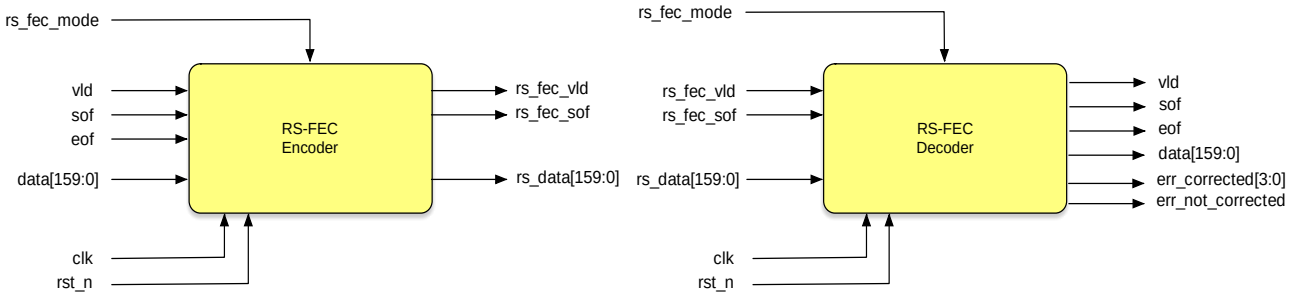
The decoder accepts sixteen 10-bit words (160 bit total) on every clock cycle when rs_vld is asserted. Additional rs_sof input is used to mark the beginning of the RS-FEC Frame. At the decoder output together with the decoded data additional sof and eof outputs are available, which marks the beginning and the end of the RS-FEC Frame.

## Highlights

- 160-bit parallel interface
- Statistics information for RS-FEC decoder
  - FEC Align Status
  - Corrected FEC codewords
  - Uncorrected FEC codewords

All information is preliminary

## Block Diagram

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