Technical Brief

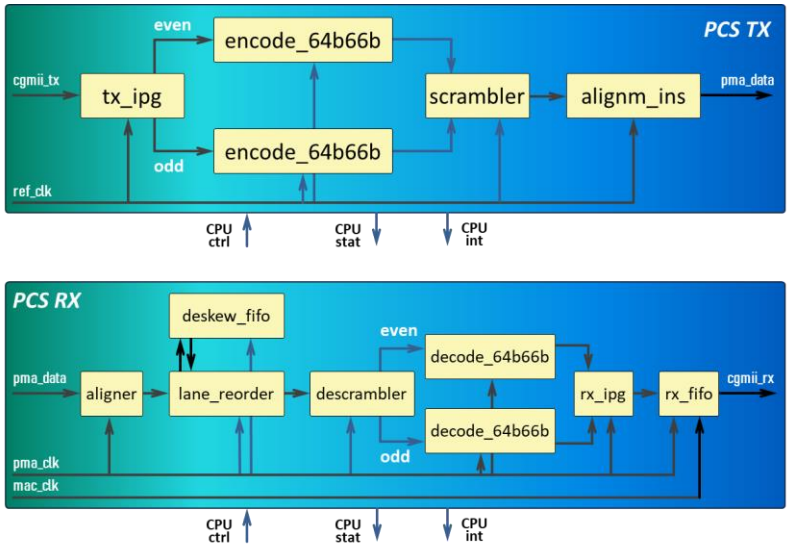
Kamaten Technology Incorporated

100G ETHERNET PHYSICAL CODING SUB-LAYER (PCS) IP CORE

Overview

This Ethernet 100G Physical Coding Sublayer (PCS) Core is designed to comply with the IEEE 803.ba specifications. It can be connected to any compatible 100G Ethernet MAC through a 128-bit Medium Independent Interface (CGMII) at core side and 132 bits generic PMA/RS-FEC Interface at lane side.

Block Diagrams



Highlights

- 100G PCS core compliant with IEEE 802.3ba Specification
- 64b/66b encoding/decoding transmit and receive PCS
- Scrambling/Descrambling using 802.3ba specified polynomial x58+x39+1
- Multi-Lane Distribution (MLD) across 20 virtual lanes for 100Gbps operation
- Periodic Alignment Marker Insertion (AM) on the transmit path and deletion on the receive path
- Skew compensation logic in order to realign all the virtual lanes and reassemble an aggregate 100G stream (with all 64b/66b blocks in the correct order)
- Lane reordering to support reception of any virtual lane on any physical lane
- BIP-8 insertion/checking per Virtual Lanes on transmit/receive respectively
- Implements Inter Packet Gap (IPG) Insertion/Deletion for Alignment Marker Compensation while maintaining a minimum of 1 byte IPG
- Near-end and far-end loopback logic
- Additional statistic implemented for various statistics required by the IEEE 802.3ba such as block synchronization status, AM lock status, lane deskew and lane reordering status and BIP-8 error counters per virtual lane

All information is preliminary

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